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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,039	09/30/2003	John K. Walton	EMC2-116AUS	5415

45456 7590 01/13/2005

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EXAMINER	
INOA, MIDYS	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,039	WALTON ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being obvious over Dobecki (6,611,879) in view of Arimilli et al. (2003/0009643).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or

subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding Claim 1, Dobecki discloses a system 100 (Figure 2) comprising:

a plurality of front end directors adapted for coupling to a host computer/server ($180_1 - 180_{32}$);

a plurality of back end directors adapted for coupling to a bank of disk drives ($200_1 - 200_{32}$);

a data transfer section 240 having cache memory 220, the cache memory being coupled to the plurality of front end and back end directors;

wherein the front end and back end directors control data transfer between the host computer/server and the bank of disk drives, such data passes through the cache memory in the data transfer section as such data passes between the host computer and the bank of disk drives (Column 5, lines 25-65);

the system of Dobecki is part of a packet switching network 260 **and the components of the system are interconnected through this network (See Figure 2).**

Dobecki also discloses the cache memory 220 receiving queries from the plurality of directors and having a resident cache management table (map maintaining a relationship...), which it uses to process the queries from the directors and determine if the requested data is in the cache (Column 6, lines 5-40)

Dobecki does not disclose a **cache memory manager** comprising the map of the relationship between cache data and disk data and determining if requested data is present in the cache.

Arimilli et al. discloses a cache memory 132 with a cache memory manager (comprised of components 134, 150, and 140) having therein a memory for storing a map maintaining a

relationship between data stored in the cache memory and data stored in the disk drives (cache directory 140, see Figure 4);

wherein the cache memory manager (see Figure 2) determines whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory (hit/miss signal 148, see Page 5, paragraph 61);

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a memory manager as that of Arimilli et al. in the system of Dobecki since memory management units provide an interface between components and support the mapping of physical to logical addresses (se Microsoft Dictionary, pg. 334 for support).

In combining the inventions of Dobecki and Arimilli, the cache memory manager, plurality of front end directors, plurality of back end directors and cache memory would be integrated into one system and all would be interconnected through the packet switching network of Dobecki. Additionally, the memory manager of Arimilli would provide an interface between the host computer, the bank of disk drives, and the cache memory for the newly formed system. **In adding the cache memory manager, the directors would no longer query the cache memory, but the queries would instead be handled by the cache memory manager.**

Regarding Claim 2, Dobecki in view of Arimilli et al. discloses the system recited in claim 1. In the invention of Dobecki in view of Arimilli, the cache memory manager must be disposed or connected to at least one of the back end directors in order to obtain data from the disk drives when such data is not present in the cache (Page 5, paragraph 061).

Regarding Claim 3, Dobecki in view of Arimilli et al. discloses the system recited in claim 1. In the invention of Dobecki in view of Arimilli the memory in the cache memory

manager 140 has a plurality of, n, locations 144, each one of the locations corresponding to a location in the disk drives, each one of the locations in the memory in the cache memory manager being adapted to store therein a disk address and an indication as to whether data stored or to be stored in such disk location is in the cache memory (Page 5, paragraph 056-057).

Regarding Claim 4, Dobecki in view of Arimilli et al. discloses the system recited in claim 3. In the invention of Dobecki in view of Arimilli the logical disk address provided by the host computer/server is hashed (page 3, paragraph 041) and the memory in the cache memory manager comprises a plurality of, m, tables 142, each one of such m tables has a plurality, n_m, locations 144 where the sum of the locations of the m tables equals n (Figure 4).

Regarding Claim 5, Dobecki in view of Arimilli et al. discloses the system recited in claim 4. In the invention of Dobecki in view of Arimilli the cache memory manager, in response to a query of the memory (store in request queue 134) therein provides an indication as to whether data stored or to be stored in such disk location is in the cache memory (hit miss signal 148) and the hashed logical disk address (page 3, paragraph 041) provided by the host computer/server is fed to address one of the m tables in the cache memory manager (page 5, paragraph 061).

Regarding Claim 6, Dobecki in view of Arimilli et al. discloses the system recited in claim 1. In the invention of Dobecki in view of Arimilli the system interface created by the cache memory manager includes a message network (Dobecki's message network 260), such message network operating independently of the data transfer section and being coupled to the plurality of front end and back end directors via a crossbar switch, the front end and back end directors for controlling data transfer between the host computer/server and the bank of disk

drives in response to messages passing between the front end directors and the back end directors through the messaging network to facilitate data transfer between host computer/server and the bank of disk drives, such data passing through the cache memory in the data transfer section as such data passes between the host computer and the bank of disk drives (Column 5, line 25 – Column 6, line 4).

Response to Arguments

3. Applicant's arguments filed on 10/25/2004 have been fully considered but they are not persuasive.

Applicant argues that Arimilli does not disclose a cache memory manager adapted to receive queries from the plurality of directors. However, the Arimilli reference is relied upon for providing the existence of a cache memory manager. **Dobecki discloses the cache memory 220 receiving queries from the plurality of directors and having a resident cache management table (map maintaining a relationship...), which it uses to process the queries from the directors and determine if the requested data is in the cache (Column 6, lines 5-40). In combining the invention of Dobecki with that of Arimilli and including the cache memory manager, the directors would no longer query the cache memory, but the queries would instead be handled by the cache memory manager.**

Applicant also argues that the elements of the invention of Dobecki are not connected to the switching network. However, the system of Dobecki is part of a packet switching network 260 **and the components of the system are interconnected through this network (See Figure 2).**

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

1/10/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER